NIKON PRECISION INC.

Double Patterning - lithography & cost considerations

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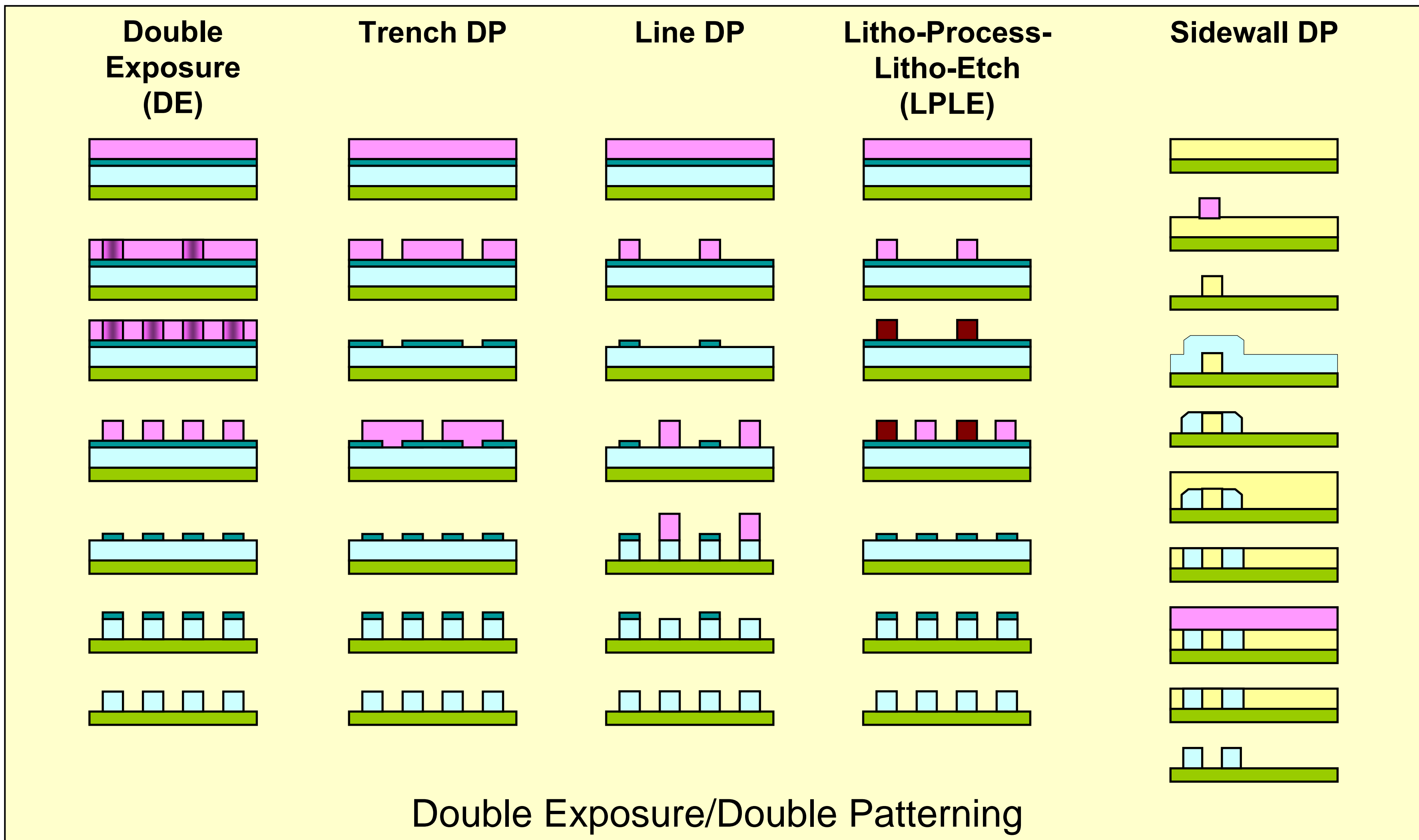
Sokudo Breakfast

Semicon, 2008

Outline

- Double patterning techniques
- CD & overlay for double patterning
  - What do we need?
  - Where are we now?
- Lithography process window considerations
- Cost of ownership for double patterning
  - Scanner throughput
  - Mask & volume considerations
- Summary

Candidate technologies – 32nm HP



The above description is an example only and should not be taken as an instruction for using our device in particular manner.

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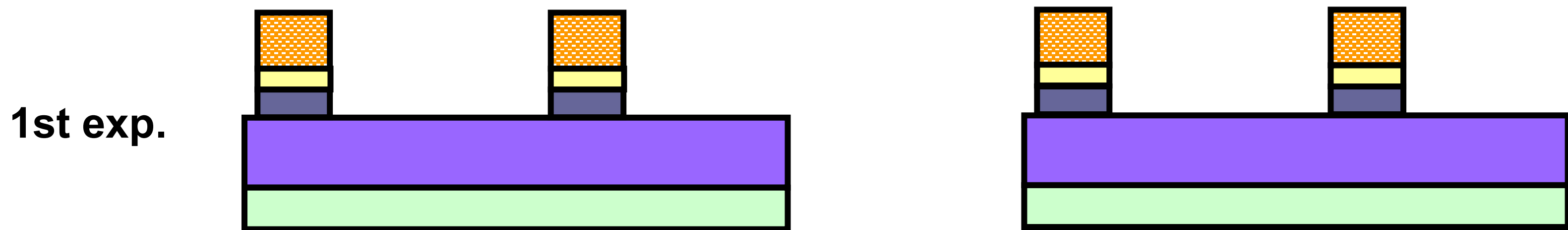
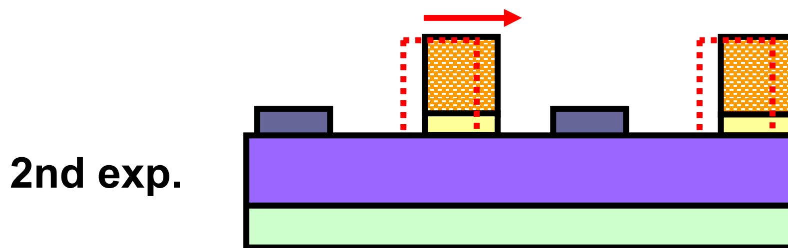
CD and overlay errors with DP

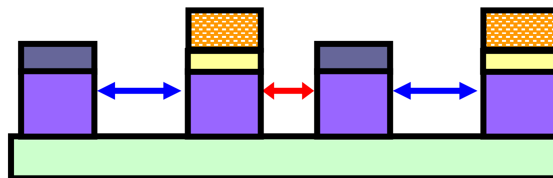


Overlay error

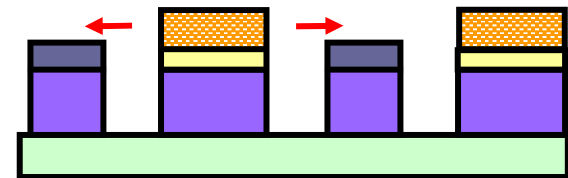


CD error

CD error



Position error



Overlay error
→ Space CD error

CD error
→ Space position error

ΔCD and overlay for pitch splitting

	Budget Spec	Line CDU	Space CDU
$\overline{L_1} - \overline{L_2}$	0.5 nm	2.6 nm	3.3 nm
ΔCD	2.5 nm		
$\overline{m_{SO}}$	0.5 nm		
ΔOL_{Line}	2.3 nm		

Δ CD requirements

ITRS Budget for
32 nm node (2013) :
3.3 nm

	Budget Spec	ΔOL_{Line}
$\overline{m_{SO}}$	0.5 nm	
ΔOL_{SO}	1.8 nm	2.3 nm
$\Delta OL_{reticle}$	1.0 nm	
$\Delta OL_{process}$	1.0 nm	
$\overline{m_{SO}} + \Delta OL_{Line}$	**2.8 nm**	

Overlay requirements

ITRS Budget for 32 nm
node: 6.4 nm →
4.5 nm for tool
Requirement for CDU :
2.8 nm

All of these numbers are challenging

S610C System Performance

	S610C
Maximum NA	1.30
Resolution	≤ 45 nm
Single Machine Overlay	≤ 6.5 nm
Throughput (300mm wafer)	≥ 130 WPH

S610Cs began shipping in early 2007

Current S610C CD uniformity stability

Scan speed: 500 mm/sec

Illumination Condition: NA 1.30, σ = 0.98, Cross Pole

CD measurement tool: CD-SEM

Interfield 3σ : 0.83 ~ 1.16 [nm]

CD deviation within wafer (nm)

5
4
3
2
1
0

CD average within wafer (nm)

100
90
80
70
60
50
40
30
20
10
0

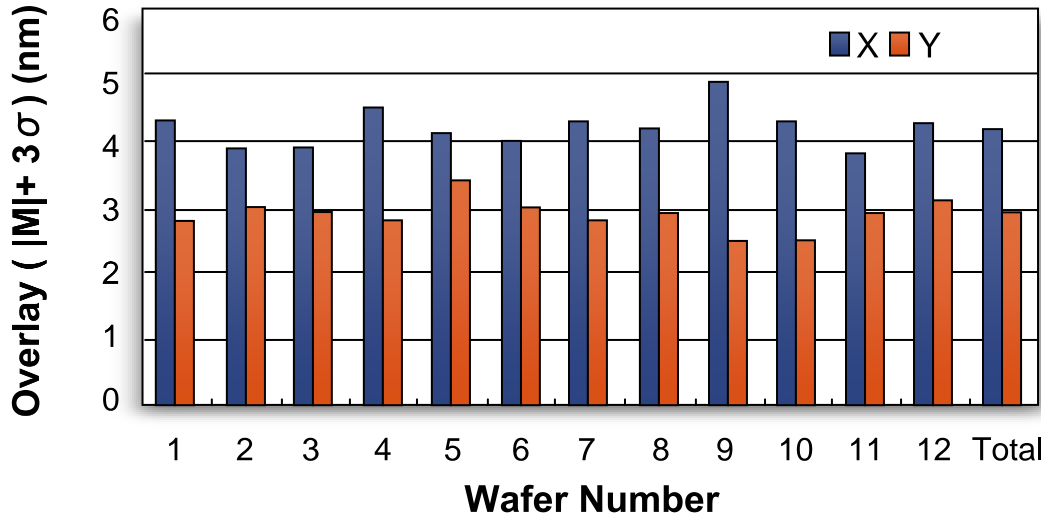
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

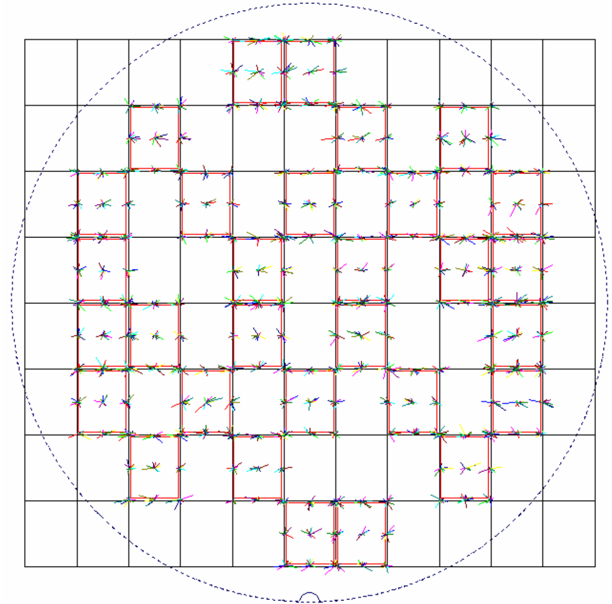
Wafer No.

Frequent calibrations ensure optimal CD uniformity and stability

Current S610C champion overlay

Single Machine Overlay



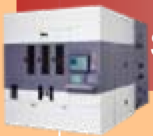


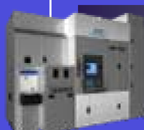
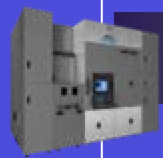
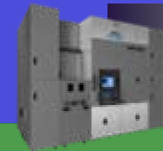
	X (nm)	Y (nm)
Overlay (|M|+ 3σ)	4.2	2.9

* standard performance 6.5 nm

Exceeds performance needed for 45 nm, and is close to meeting DP requirements

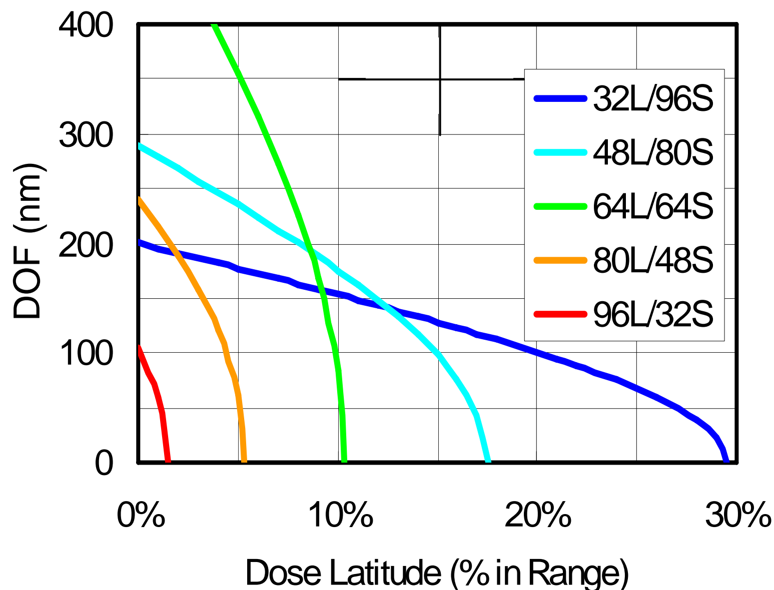
Technology Generation		2006	2007	2008	2009	2010
280 nm	i-line	SF140	SF150 NA 0.62 Stepper	Skyhook Technology		
				SF155 NA 0.62 TP Enhance	Skyhook technology	
150 nm / 110 nm	KrF	S208D NA 0.82 Scanner		S210D NA 0.82 Scanner	Tandem Stage	
90 nm / 65 nm	ArF	S308F NA 0.92 Scanner		S310F NA 0.92 Scanner	Tandem Stage	
55 nm	ArFi	S609B NA 1.07 Immersion Scanner	Tandem Stage			
45 nm			S610C NA 1.30 Immersion Scanner	Tandem Stage		
32 nm						S6XX DP Immersion Scanner
22 nm	EUVL	EUVA ASET Program		EUV1 NA 0.25		EUV2

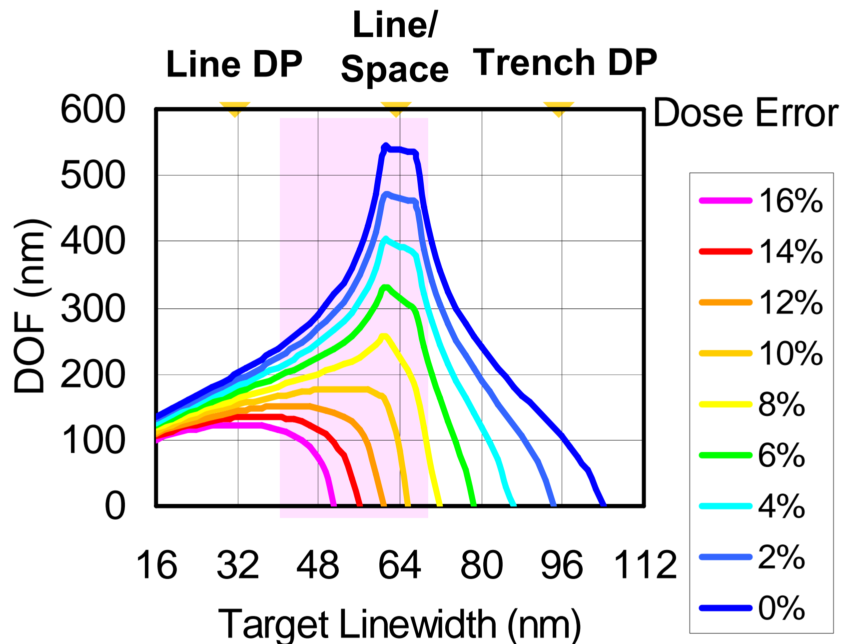


Process window simulations

- **Simulation conditions**
  - **Expose 128 nm Pitch L/S**
  - **Mask Error: ΔM=+/-1nm**
  - **CD Error: ΔCD=+/-1.6nm(5% of 32 nm)**
  - **Process window & DOF dependency on Target size**





Imaging performance for Line/Space with process assist is acceptable.

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Comparison of DP techniques

Trench DP

Line / Space

Line DP

1st Exp.

Sidewall Process

Resist Slimming

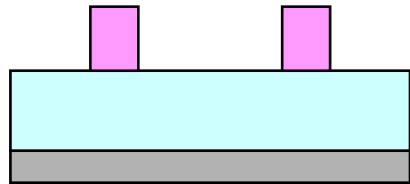
2nd Exp.

Finish

Sidewall process

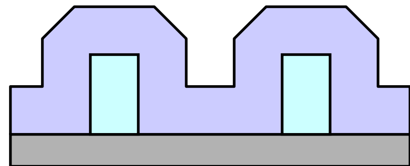
Principle of Sidewall Process

Expose

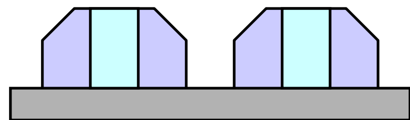


Underlayer Etching

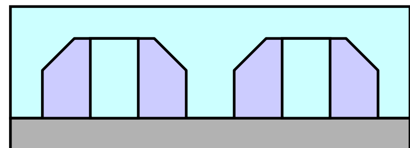
Isotropic CVD
Thickness →CD



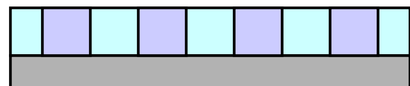
Anisotropic Etching



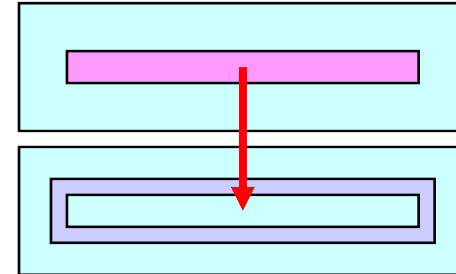
2nd CVD



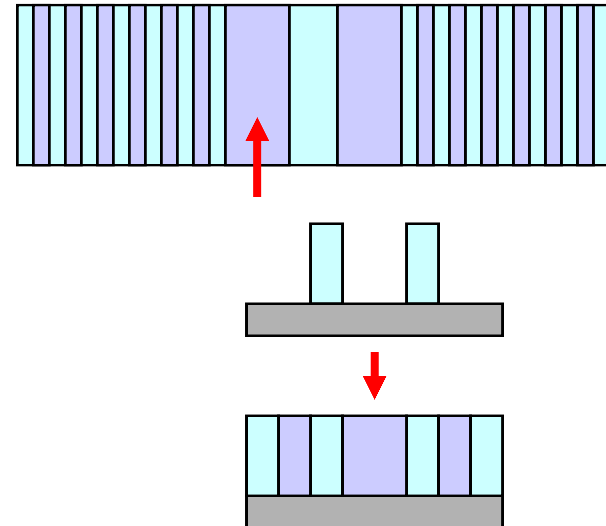
CMP



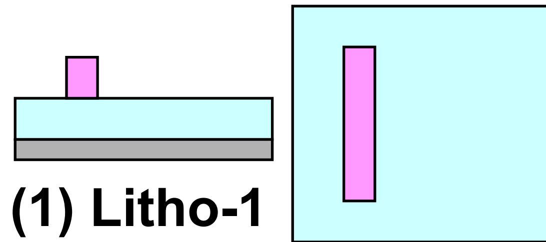
Problem 1 – Print “Open” Pattern

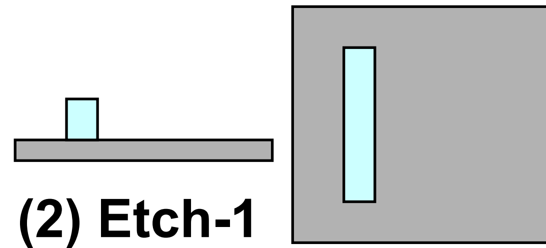


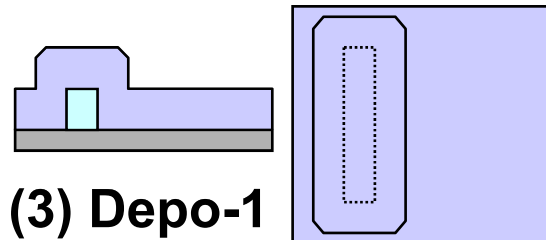
Problem 2 – Print “Thick” Pattern

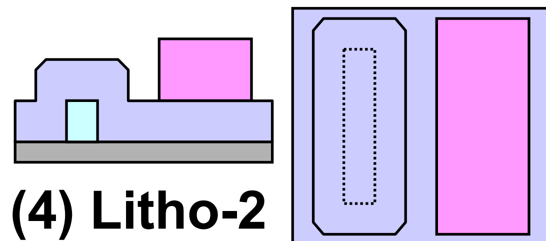


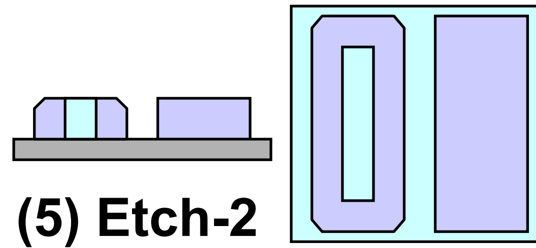
Sidewall process flow estimate

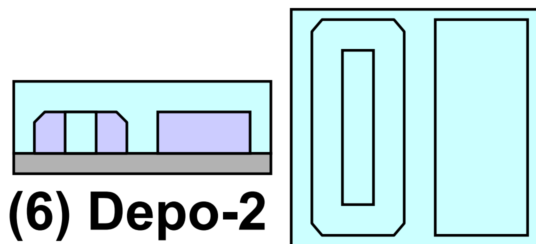


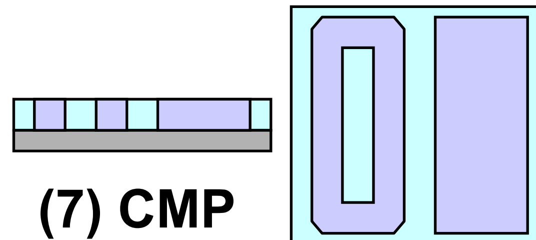


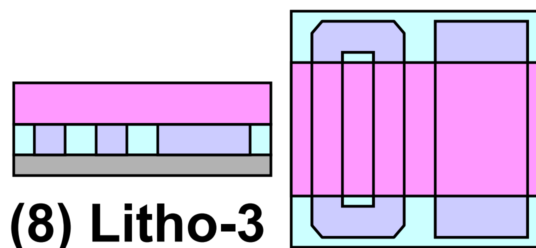


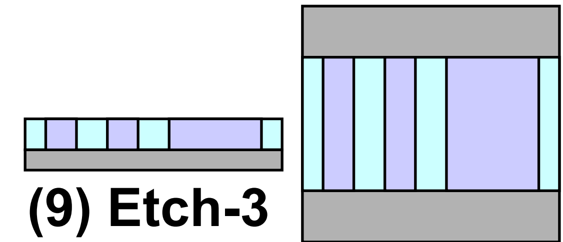


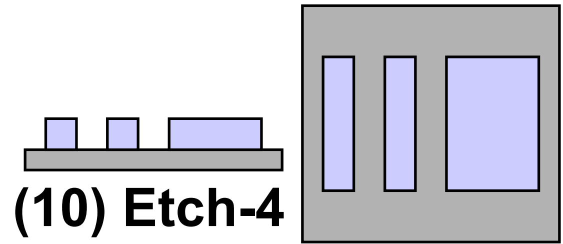












Both line-end and thick-line are possible.

Application for more complex patterns could be difficult

Throughput and CoO for DP

- What effects throughput and CoO for DP?
  - Raw throughput
  - Number of process steps
  - Complexity of process steps
  - Number of pieces of equipment
  - Complexity of equipment / # modules
- Plus, long cycle times could be difficult to manage

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Potential process steps

		45nm SE	32nm DE	32nm Trench DP	32nm Line DP	32nm LPLE (Freeze)	32nm sidewall
Deposition	Hard Mask	1	1	1	1	1	0
	Base Layer	1	1	1	1	1	3*
Litho		1	2 (1)	2	2	2	2
Coat / Develop / Bake		1	1	2	2	2	2
Metrology		1	1	2	2	1	2
Etch	Hard Mask	2 (1)	2 (1)	3 (2)	2 (2)	2 (1)	0 (3)
	Base Layer	1	1	1	1	1	4*
Clean		1	1	2	2	1	2
CMP							1

(1) : number of passes through tool

* : includes sacrificial layer

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32nm DP cost comparison

20,000 wafers/mask

Sidewall most expensive due to deposition and etch costs

3.0
2.5
2.0
1.5
1.0
0.5
0.0

45 nm SE (125 wph)
32 nm DE (90 wph)
32 nm Trench DP (180 wph)
32 nm Line DP (180 wph)
32 nm LPLE (180 wph)
32 nm Sidewall DP (180 wph)

- Other CoO
- Etch CoO
- Reticle CoO
- Litho (excl. Reticle) CoO
- Deposition CoO

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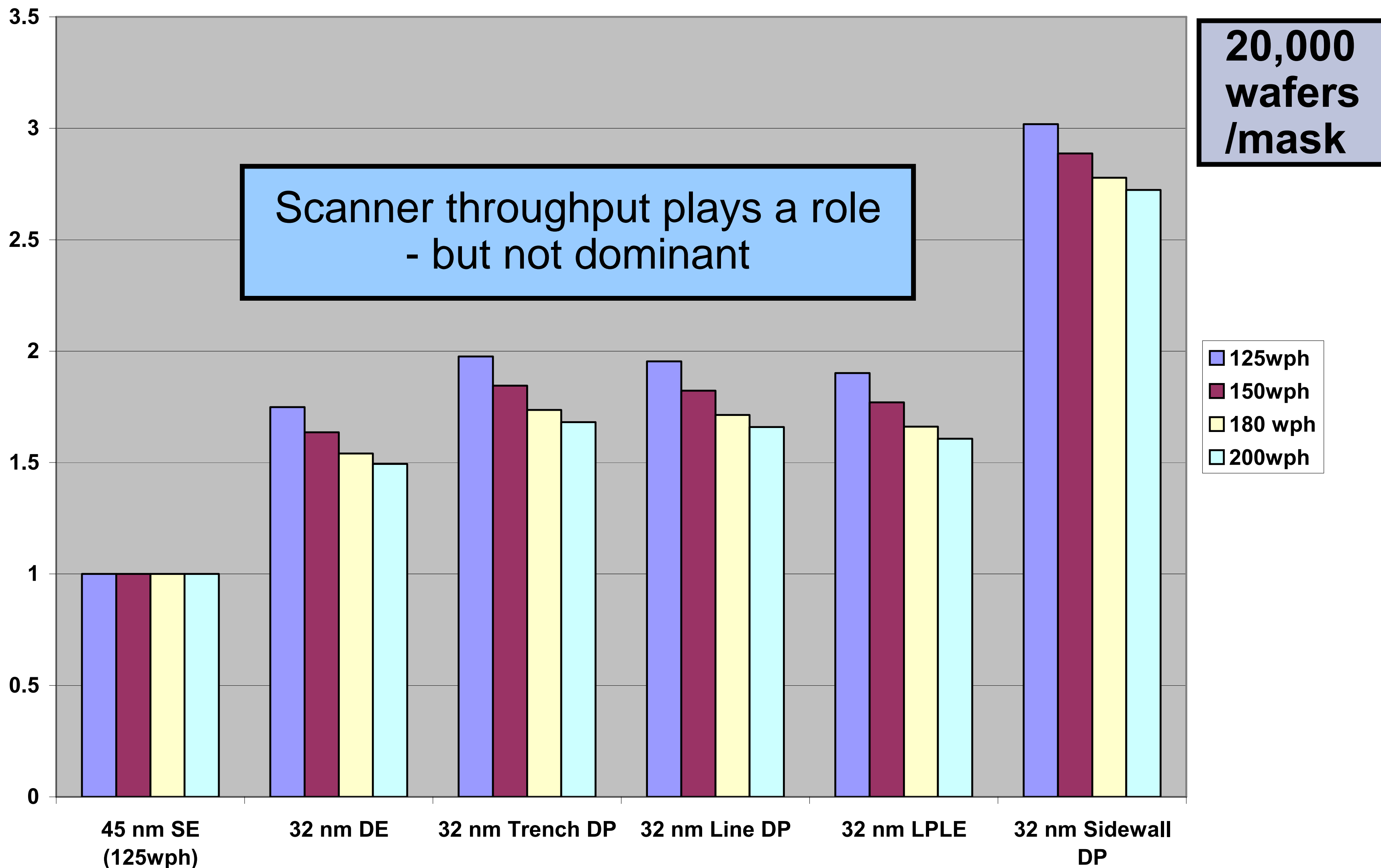
Scanner throughput & total CoO



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32nm DP costs – 20,000 wafers/mask

8
7
6
5
4
3
2
1
0

45 nm SE (125 wph)
32 nm DE (90 wph)
32 nm Trench DP (180 wph)
32 nm Line DP (180 wph)
32 nm LPLE (180 wph)
32 nm Sidewall DP (180 wph)
32 nm EUV (100 wph)

- Other CoO
- Etch CoO
- Reticle CoO
- Litho (excl. Reticle) CoO
- Deposition CoO

EUV tool & consumables cost high

32nm DP costs – 2,000 wafers/mask

Summary

- Double patterning is the most likely candidate for 32 nm HP dense features
- Requirements on the lithography process will be severe, but are within reach
- Device makers will likely use alternative technologies to avoid the most severe requirements
- Cost of ownership for DP is dependent on process complexity and volume
- Nikon is developing exposure tools to satisfy double patterning and alternate methods

Acknowledgements

- Andy Hazelton
- Bernie Wood

and of course, our hosts :

SOKUDO

Thank You